In the Specification

Please amend the specification of this application as follows:

Rewrite the paragraph at page 3, lines 3 to 9 as follows:

--The early direct memory access has evolved into several successive versions of centralized transfer controllers and more recently into the transfer controller with hub and ports architecture. The transfer controller with hub and ports architecture is described in U.K. Patent Application No. 9909196.9 filed April 10, 1999 entitled "TRANSFER CONTROLLER WITH HUB AND PORTS ARCHITECTURE" ~~(TI-28983)~~ now U.S. Patent No. 6,496,740.--

Rewrite the paragraph at page 5, lines 2 to 9 as follows:

--The transfer controller with hub and ports has undergone significant refinements in implementation that followed the original description in U.K. Patent Application No. 9909196.9 filed April 10, 1999 entitled "TRANSFER CONTROLLER WITH HUB AND PORTS ~~ARCHITECTURE."~~ ARCHITECTURE" now U.S. Patent No. 6,496,740. One such refinement is the use of a write allocation counter in the source pipeline. The algorithm upon which this write allocation counter operates is also key to the invention.--